SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. non-provisional patent application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2015-0108158, filed on Jul. 30, 2015, in the Korean Intellectual Property Office, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] 1. Field

[0003] Some example embodiments of the inventive concepts relate to a semiconductor devices and a method for manufacturing the same, and more particularly, to a semiconductor device including a field effect transistor and a method for manufacturing the same.

[0004] 2. Description of the Related Art

[0005] Semiconductor devices are widely used in an electronic industry because of their relatively small sizes, multi-functional characteristics and/or relatively low manufacturing costs. Semiconductor devices may be classified into semiconductor memory devices storing logical data, semiconductor logic devices processing logical data, and hybrid semiconductor devices having both the function of the semiconductor memory devices and the function of the semiconductor logic devices. Semiconductor devices with improved characteristics have been demanded with the development of the electronic industry. For example, relatively high-reliable, high-speed and/or multi-functional semiconductor devices have been increasingly demanded. To satisfy these demands, structures of semiconductor devices have been complicated and semiconductor devices have been highly integrated.

SUMMARY

[0006] Some example embodiments of the inventive concepts may provide a semiconductor device including a field effect transistor with improved electrical characteristics.

[0007] Other example embodiments of the inventive concepts may provide a method for manufacturing a semiconductor device including a field effect transistor with improved electrical characteristics.

[0008] According to an example embodiment, a semiconductor device includes a substrate including at least one metal-oxide-semiconductor field-effect transistor (MOSFET) region defined by a device isolation layer and having an active pattern extending in a first direction on the MOSFET region, a gate electrode intersecting the active pattern on the substrate and extending in a second direction intersecting the first direction, and a first gate separation pattern adjacent to the MOSFET region when viewed from a plan view. The first gate separation pattern may divide the gate electrode into segments spaced apart from each other in the second direction. The first gate separation pattern may have one of a tensile strain and a compressive strain when the MOSFET region is one of a P-channel MOSFET (PMOSFET) region and N-channel MOSFET (NMOSFET) region, respectively.

[0009] In an example embodiment, the MOSFET region may be the PMOSFET region, and the active pattern may have a compressive strain.

[0010] In an example embodiment, the MOSFET region may be the NMOSFET region, and the active pattern may have a tensile strain.

[0011] In an example embodiment, a bottom surface of the first gate separation pattern may be at a lower level than a bottom surface of the gate electrode.

[0012] In an example embodiment, the first gate separation pattern may be on the device isolation layer, and a bottom surface of the first gate separation pattern may be at a lower level than a topmost surface of the device isolation layer.

[0013] In an example embodiment, a top surface of the first gate separation pattern may be at the same level as a top surface of the gate electrode.

[0014] In an example embodiment, the first gate separation pattern may extend in the first direction.

[0015] In an example embodiment, the semiconductor device may further include a second gate separation pattern dividing the gate electrode into segments spaced apart from each other in the second direction. The first and second gate separation patterns may be spaced apart from each other with the MOSFET region therebetween and the second gate separation pattern may be adjacent to the MOSFET region when viewed from a plan view. The second gate separation pattern may have a tensile strain when the MOSFET region is the PMOSFET region, and the second gate separation pattern may have a compressive strain when the MOSFET region is the NMOSFET region.

[0016] In an example embodiment, the MOSFET region may include a first MOSFET region and a second MOSFET region spaced apart from each other in the second direction. The first MOSFET region may correspond to the PMOSFET region and the second MOSFET region may correspond to the NMOSFET region. The first gate separation pattern may be adjacent to the first MOSFET region and the second gate separation pattern may be adjacent to the second MOSFET region. In this case, the first gate separation pattern may have the tensile strain and the second gate separation pattern may have the compressive strain.

[0017] In an example embodiment, the device isolation layer may extend between the first MOSFET region and the second MOSFET region, and the semiconductor device may further include a third gate separation pattern on the device isolation layer between the first MOSFET region and the second MOSFET region.

[0018] In an example embodiment, a distance between the third gate separation pattern and the first MOSFET region may be less than a distance between the third gate separation pattern and the second MOSFET region, and the third gate separation pattern may have a tensile strain.

[0019] In an example embodiment, a distance between the third gate separation pattern and the second MOSFET region may be less than a distance between the third gate separation pattern and the first MOSFET region, and the third gate separation pattern may have a compressive strain.

[0020] According to another example embodiment, a semiconductor device includes a substrate including an active pattern extending in a first direction, a gate electrode intersecting the active pattern on the substrate and extending in a second direction intersecting the first direction, source/drain regions on the active pattern at both sides of the gate electrode, and a gate separation pattern adjacent to the active pattern when viewed from a plan view. The gate separation pattern may divide the gate electrode into segments spaced